Characterization of Linear and Nonlinear Properties of GaAs MESFET's for Broad-Band Control Applications

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Abstract—**GaAs MESFET's designed for control applications have improved switching performance compared to FET's designed for low-noise or high-power amplifiers. A broad-band switching cutoff frequency figure of merit close to 500 GHz has been achieved with both epitaxial and ion-implanted devices having n^+ surface layers and/or channel dopings above 2.0×10^{17} cm^{-3}. Power handling under CW conditions is limited in the nonconducting state (FET dc biased into pinchoff) by the difference between the gate breakdown voltage and the pinchoff voltage, while conducting-state power handling is limited by the open-channel current-handling capability. For optimum switching frequency figure of merit, individual gate finger widths greater than those used in amplifier devices for the same maximum frequency of operation are necessary. The large (~ 5 kΩ) resistor in series with the gate has important ramifications in optimizing the power-handling capability for broad-band applications.**

I. Introduction

GALLIUM-ARSENIDE MESFET's are becoming recognized as viable RF control devices for applications such as switching and phase shifting, particularly in microwave monolithic integrated circuit (MMIC) implementations. Passive MESFET two-state control components have low bias power consumption (~ 10 μW dependent upon Schottky gate leakage) and fast switching times (~ 1 ns dependent upon the gate bias circuit RC time constant and the driver circuitry) [1]. Moreover, multioctave bandwidth capability can be achieved since the dc bias terminal (gate) and the RF terminals (source and drain) are easily isolated resistively (with an ion-implanted resistor) without significant dc or RF power dissipation.

The inherent disadvantages of GaAs MESFET's in passive control applications compared to conventional Si p-i-n diodes are twofold: 1) lower switching cutoff frequency figure of merit and 2) lower power-handling capability. This paper describes an approximate switching figure of merit for broad-band (baseband or near-baseband to 10 or 20 GHz) control applications, presents an approximate analysis of the CW power-handling limitations of FET control components, and provides data on a variety of FET's evaluated for control applications (both discrete epitaxial and ion-implanted monolithic devices). Finally, we present some differences between MESFET's designed for control functions and those used in more typical amplifier applications.

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II. Broad-Band Control Performance Parameters

In comparing the control component capabilities of alternative two-states devices, the switching cutoff frequency figure of merit is useful to compare low-power performance determined by device linear characteristics [2]. Although adapted by others into forms appropriate for specific applications of FET switches [3], [4], a more simplified version is useful for broad-band applications. Considering the intrinsic FET small-signal equivalent circuits presented in Fig. 1, the simplified representations hold for reasonable devices characteristics in the frequency range suitable for broad-band applications. Since the nonconducting-state (with the dc voltage applied to the gate relative to the dc-connected source and drain greater than the pinchoff voltage $|V_G| > V_p$) resistance R_{NC} is less than the conducting-state (gate dc-shorted to the source and drain $|V_G| = 0$) resistance R_C, the switching $\hat{Q}$ and the switching cutoff frequency figure of merit f_{cs} can be approximated as

$$\hat{Q} = \frac{|Z_C - Z_{NC}|}{(R_C R_{NC})^{1/2}} > \frac{|Z_C - Z_{NC}|}{R_C} \approx \frac{1}{\omega C_{NC} R_C}$$

$$f_{cs} = \frac{1}{2\pi C_{NC}(R_C R_{NC})^{1/2}} > \frac{1}{2\pi C_{NC} R_C}.$$

Since the nonconducting-state resistance R_{NC} is more difficult to experimentally determine with precision and is less important than R_C and C_{NC} in broad-band applications, the broad-band switching cutoff figure of merit is approximated by this lower bound, namely

$$f_{cs_{BB}} \approx \frac{1}{2\pi C_{NC} R_C}.$$

A device structure that provides the minimum $R_C C_{NC}$ product is capable of best broad-band control component performance, with the required R_C–C_{NC} tradeoff obtained

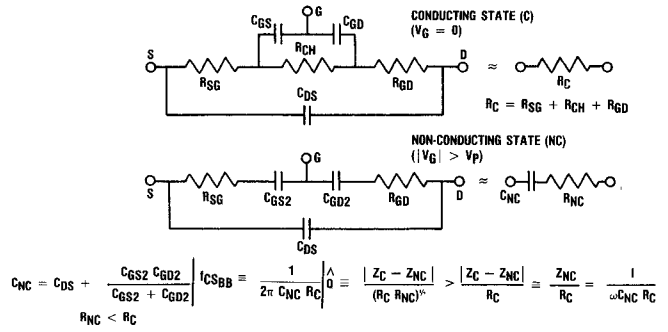

Fig. 1. Intrinsic GaAs MESFET control device equivalent circuit.

by varying the total gate periphery W (gate finger width times number of fingers).

Unfortunately, the power-handling capability of broad-band FET control components cannot be as easily summarized by a single parameter. Assuming power handling is required in both states, the power-handling capability of a control device is usually considered to be determined by the $V_m I_m$ product [5], where V_m is the maximum value of the rms RF voltage that can be handled in the nonconducting state and I_m is the maximum value of the rms RF current that can be handled in the conducting state. However, the usefulness of this product depends upon a necessary flexibility in the design of the switching circuit, either by adjusting parameter values such as characteristic impedance or by selecting alternative circuit topologies. Such flexibility does not usually occur in broad-band MMIC design.

Therefore, we will focus on the specification of both V_m, the maximum value of the rms RF voltage that can exist across the source–drain terminals in the nonconducting state (dc value of gate voltage $|V_G| > V_p$), and I_m, the maximum value of the rms RF current that can pass through the FET conducting channel in the conducting state ($V_G = 0$). Both V_m and I_m are affected by the Schottky gate and the value of resistor in series used to isolate the bias and RF terminals as described later in this paper. Specifically, the control FET exhibits nonlinear resistive characteristics in the nonconducting state when either the Schottky gate enters avalanche breakdown or the channel is not completely pinched off during part of the RF cycle, thus limiting V_m. In the conducting state, I_m is limited by the ability of the conducting channel to transport current without domain formation or by the ability of the Schottky gate circuitry to sink additional RF current.

III. MESFET Parameters and Linear Control Device Characteristics

Seven sets of devices were measured, with gate lengths varying from 0.3 to 1.0 μm, gate peripherics from 400 to 1200 μm, and pinchoff voltages from 2 to 6 V. Both discrete FET's fabricated with vapor phase epitaxial channels and monolithic FET's fabricated with ion-implanted channels were tested. Although the earlier FET's have device parameters typical of low noise, signal, or power amplifier devices, particular emphasis was placed on

TABLE I
Approximate Characteristics of GaAs MESFET's Evaluated

DEVICE TYPE	l_g (μm)	W (μm)	V_p (VOLTS)*	l_{gs} (μm)	l_{gd} (μm)	N_D (cm^{-3})
A	0.8	400	3	1.7	1.7	2 x 10^{17}
B	1.0	1200	3-5	1.8	2.5	1 x 10^{17}
C	0.3	400	3-6	1 5	1.5	1.6 x 10^{17}
D	0.3	400	1.5-2.5	1.4	1.4	3 4 x 10^{17}
E	1 0	1200	4-5	1.5	1.5	1.1 x 10^{17}
F	1.0	530	3-4	1.5	1.5	1 2 x 10^{17}
G	0.5	530	2-3	1 5	1 5	2.4 x 10^{17}

*Range of pinchoff voltages tested.
Devices A–D: discrete FET's fabricated with vapor phase epitaxial channels.
Devices E–G: monolithic FET's fabricated with ion-implanted channels.

TABLE II
GaAs MESFET Control Characteristics

DEVICE TYPE	R_C (OHMS)	C_{NC} (pF)	f_{SW} (GHz)	I_{DSS} (mA)	V_{brG} (V)	P (WATTS)*
A	5.5	0.09	320	100	18	.25/1.5
B	4.0	0.17	230	230	20	1.0/2.5
C	7.5	0.07	300	90	13	0.25/1.0
D	6.1	0.06	435	80	11	0.25/1.0
E	2.6	0.32	190	220	20	1.0/2.5
F	6.6	0.08	290	155	15	0.5/1.5
G	4.2	0.08	470	90	14	0.25/1.0

*CW power performance in a series SPST switch. The lower values correspond to the onset of reversible nonlinear characteristics; the upper value is the maximum power-handling capability.

TABLE III
Normalized Conducting-State Resistances, Nonconducting-State Capacitances, and Broad-Band Switching Figure of Merit

DEVICE TYPE	$R_C W$ ohm-mm	$\frac{C_{NC}}{W}$ pF/mm	f_{csBB} GHz
A	2.2	.23	320
B	4.8	.14	230
C	3.0	.18	300
D	2.4	.15	435
E	3.1	.27	190
F	3.5	.16	290
G	2.2	.15	470

evaluation of high-pinchoff-voltage and/or high-channel-doping devices as being more desirable from a switching-frequency figure-of-merit criterion. The complete set of device characteristics is presented in Table I. All devices are fabricated with recessed gates, and device types A, C, and D have n^+ surface layers in the regions between source-and-gate and drain-and-gate.

The nominal performance of these seven device types is presented in Table II. In general, R_C is lower with large gate periphery, high channel doping, short gate length and source-to-drain spacings, high pinchoff voltage, and with an n^+ surface layer. As described previously [1], [3], [4], the conducting-state resistance is limited by the FET structure and by the conducting path from source to drain at zero gate bias. A value of $R_C W$ varying from 2.2 to 4.8 $\Omega \cdot$ mm was obtained in these devices (Table III).

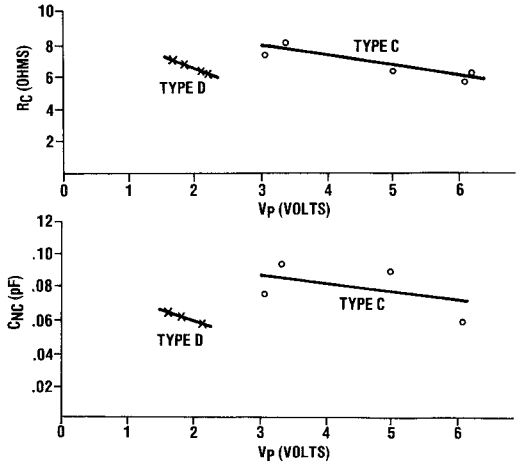

Fig. 2. R_C and C_{NC} dependence upon pinchoff voltage for FET types C and D.

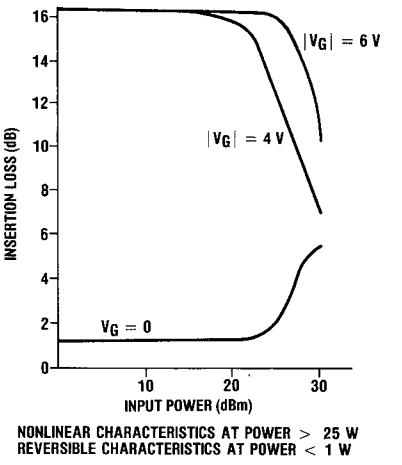

Fig. 3. Power-handling capability of device type D in SPST series switch.

The dependence of R_C and C_{NC} on pinchoff voltage (varied principally by channel thickness) is shown in Fig. 2 for device types C and D. The advantage of a thicker conducting channel in reducing R_C is observed, and the decrease in C_{NC} with increasing channel height is attributed to a reduced sidewall capacitance. For the devices tested, C_{NC}/W values varied from 0.14 to 0.27 pF/mm. The broad-band switching frequency figure of merit ($f_{cs_{BB}}$) varied from 190 to 470 GHz for the devices evaluated (Table III).

IV. Nonlinear Control Device Characteristics and Power Handling

The power-handling capability of these devices in a SPST series or shunt switch varies from 1.0 to 2.5 W as defined by an irreversible change in device parameters. However, the devices exhibit a reversible, nonlinear change in resistance at lower power levels, varying from 0.25 to 1.0 W, as presented in Table II for the series configuration. Fig. 3 illustrates typical nonlinear behavior for device type D in a series configuration. The nonlinear nonconducting-state characteristics can be extended to higher power levels by proper gate bias selection, i.e., between $1/2(V_{brG}+V_p)$ and V_{brG} or 8 to 14 V for the FET depicted later in this section. For practical purposes, this FET has a 0.25-W power-handling capability in the SPST switch, since the strong nonlinear behavior between 0.25 and 1.0 W will not be tolerable in most applications.

The nonlinear characteristics were investigated in detail by mounting discrete FET's in shunt with a 50-Ω transmission line, measuring the transmission and reflection characteristics versus incident power, and calculating device RF parameters. Fig. 4 depicts the dependence of the shunt resistance (6.1 Ω at low power), RF peak voltage across the FET (V_{ds}) and RF peak current through the drain (I_d) upon incident power level at 5.0 GHz.

From these results, we conclude that the initial nonlinear resistive behavior occurs when the RF current amplitude approaches the saturation current of the FET I_{DS} ($I_{DS}=82$ mA at $V_{GS}=0$ and $I_{DS}=110$ mA at $V_{GS}=+0.5$

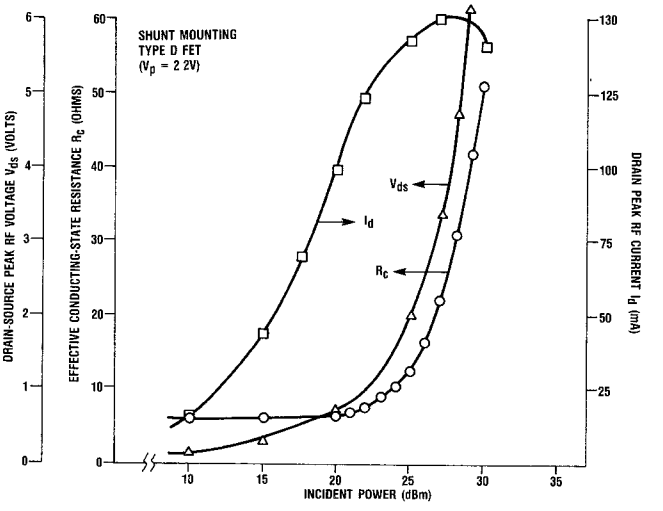

Fig. 4. Nonlinear characteristics of shunt-mounted SPST switch (type D FET) in conducting state.

V for the FET shown in Fig. 4). We believe that a Gunn domain is formed at this power level in an attempt to handle more RF current, as the transmission and reflective phase angles change slightly (5° to 10°) in this power range, indicative of additional device capacitance.

At slightly higher power levels, the RF voltage in the conducting channel approaches the value to cause gate conduction during part of the RF cycle. For the device of Fig. 4, we expect that gate conduction begins at $V_{ds}=1.1$ V (accounting for parasitic voltage drops outside the channel region). While gate conduction tends to sink more current to ground, the ion-implanted gate isolation resistance tends to inhibit appreciable gate conduction (although there is gate rectification and a finite dc gate voltage developed). Higher RF current-handling capability is feasible if the gate circuitry allows additional current sinking to ground.

We expect that the I_d-V_{ds} RF characteristics obtained are actually $I_{ds}-V_{ds}$ device curves, with a small finite dc gate voltage at higher power levels due to Schottky gate rectification. The $I_{ds}-V_{ds}$ relationship derived is shown in Fig. 5, where the 150-mA hard current saturation is consistent with the calculated open-channel current-handling

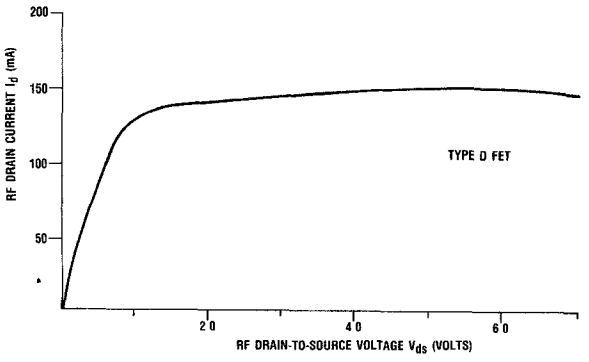

Fig. 5. FET large-signal RF characteristics in broad-band control conducting-state operation.

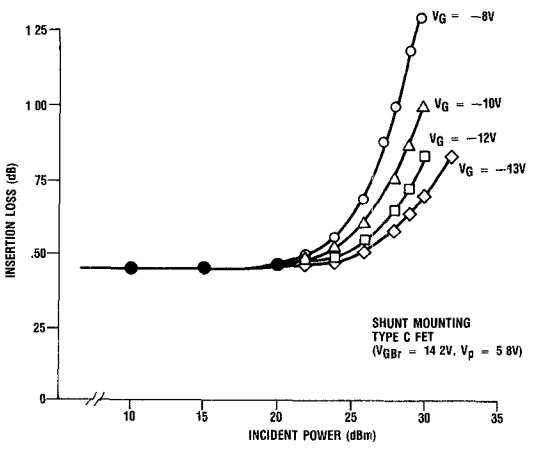

Fig. 6. Nonlinear characteristics of shunt-mounted SPST switch (type C FET) in nonconducting state.

capability of the device. Since $\omega\tau \gg 1$ at 5 GHz for both the momentum and energy relaxation time, the RF and dc high-level conductivities are expected to be equal.

In the nonconducting state, the optimum dc gate bias is usually considered to be $1/2(V_{brG}+V_p)$, that is, midway between the gate breakdown voltage and pinchoff [1]. This maximizes the RF voltage swing if both avalanche breakdown is to be prevented and channel pinchoff is maintained during the entire RF cycle. In the broad-band control application, the gate floats at $V_G+\frac{1}{2}V_{ds}$ in the linear region as a result of the gate RF isolation and device symmetry (refer to Fig. 1), consistent with the above consideration.

However, the gate isolation resistance stabilizes the avalanche condition. As the gate goes into avalanche breakdown during part of the RF cycle, the gate current pulses result in a lower negative gate bias, thus preventing a damaging amount of gate current. In fact, the negative dc gate bias can approach V_{brG} if the gate bias resistance is sufficient. While additional testing is necessary, we believe that gate bias at a magnitude of $1/4(3V_{brG}+V_p)$ is most appropriate, resulting in a maximum peak RF voltage swing of $3/4(V_{brG}-V_p)$ rather than $1/2(V_{brG}-V_p)$. This 50-percent increase in V_m results in twice the power handling in a given circuit configuration.

In fact, gate biasing near the gate breakdown voltage has been demonstrated to yield still higher linear power handling capability. A type-C FET was mounted in a shunt SPST switch topology having a pinchoff voltage of 5.8 V and a gate breakdown of 14.2 V to demonstrate the improvement. The insertion loss versus incident power is indicated in Fig. 6. If we define the power-handling capability as the power level at which the insertion loss increases by 0.4 dB, this FET can tolerate 27 dBm, 29 dBm, 30 dBm, and 32 dBm at $V_G=-8$ V, -10 V, -12 V and -13 V, respectively. The peak RF voltage across the FET ranges from 7.1 V at 27 dBm to 12.6 V at 32 dBm, indicating that the constraint of peak RF voltage swing given above is conservative. Similar results have been observed with the other device types listed in Table I, although the testing has been less extensive.

Even though this shunt-mounted device exhibits nonlinear characteristics in the conducting state at 24 dBm, the improvement in nonconducting-state power handling from 27 dBm to 32 dBm is important. The nonconducting-state voltage stress can often be traded against conducting-state current stress by circuit topology. For example, with a simple SPST switch, a shunt configuration has half the voltage stress and twice the current stress compared to a series configuration. Also, the gate periphery W can be increased to allow additional conducting-state power handling without affecting the nonconducting-state power handling (assuming device uniformity). With increased gate periphery, the broad-band switching frequency figure of merit remains unchanged (R_C decreases while C_{NC} increases). Finally, in some phased array module applications (receiver protection and some duplexer topologies) power handling is required in only one state.

V. MESFET Design Principles for Control Applications

While device design is circuit topology and application dependent, a few features of device design for broad-band control applications are generic guidelines. The key parameter in a control design is usually the conducting-state resistance R_C. For applications with modest power-handling requirements (<30 mW), more heavily doped (2–5 $\times 10^{17}$ cm^{-3}) thicker ($V_{brG} \approx V_p+5$ V) channels are preferred to minimize the gate periphery required to achieve a desired R_C. Since the control FET operates with a zero dc drain–source voltage, heavier doping and thicker channels can be utilized.

In addition, the FET channel is completely pinched off in the nonconducting state; that is, the channel is pinched off over the entire length of the gate (at least at low RF power), not only at the drain end as in an amplifier. Therefore, the lower sidewall capacitance is the dominant intrinsic gate capacitance [6], and parasitic capacitances become more critical. In fact, conventional MESFET simulation programs overestimate C_{NC} by an appreciable amount. For example, Table IV presents the experimental results and C_{NC} values calculated with FETRAN [7] for device types C and D. We typically observe 10 to 50 percent more capacitance in such device simulations.

TABLE IV
COMPARISON OF CALCULATED AND MEASURED NONCONDUCTING-STATE CAPACITANCES

	FETRAN SIMULATION (pF)	
	DEVICE TYPE D (V_p = 2.0V, N_d = 3.4 x 10^{17} cm^{-3})	DEVICE TYPE C (V_p = 4.0V, N_d = 1.6 x 10^{17} cm^{-3})
C_{GS} (external)	.034	.042
C_{GD} (external)	.034	.032
C_{SD} (external)	.074	.065
$C_{NC} = C_{SD} + \frac{C_{GS}C_{GD}}{C_{GS} + C_{GD}}$	.091	.084
C_{NC} (measured)	.06	.07

On the other hand, there is only small RF current in the gate, so that gate resistance is less critical than in an amplifier. As a result, high-frequency, broad-band control FET's of relatively large total periphery W should have a few longer gate fingers as opposed to many shorter gate fingers (as utilized in high-frequency amplifier FET's). A self-aligned gate MESFET using either refractory silicide gates [8] or pattern inverse gate technology [9] should yield optimum broad-band switching frequency figure of merit for low-power applications.

Finally, the power-handling limitations are different in broad-band control applications and are greater than amplifier devices in magnitude. As demonstrated, the peak RF current in the conducting state is comparable to the open-channel current-handling capability, unless additional current sinking to ground is provided by the gate circuitry. The maximum peak RF voltage in the nonconducting state appears comparable to the gate breakdown voltage minus the pinchoff voltage, with higher linear power handling resulting with bias near the gate breakdown voltage. For example, a power amplifier FET has a power output of approximately 0.5 W/mm of gate periphery. In general in control applications, FET's can handle approximately 2 W/mm before failure and 0.7 W/mm before nonlinear degradation in performance occurs (Tables I and II). However, with optimized device and circuit design, power handling of 2 W/mm has been achieved prior to nonlinear degradation.

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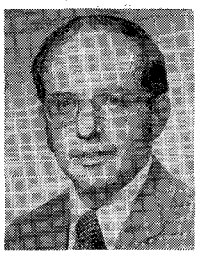
REFERENCES

[1] Y. Ayasli, "Microwave switching with GaAs FETs," *Microwave J.*, vol. 25, pp. 61–74, Nov. 1982.
[2] M. E. Hines, "Fundamental limitations in RF switching and phase shifting using semiconductor diodes," *Proc. IEEE*, vol. 52, pp. 697–708, June 1964.
[3] H. A. Atwater and R. W. Sudbury, "Use of switching Q in the design of FET microwave switches," in *IEEE MTT-S Int. Microwave Symp. Dig.*, 1981, pp. 370–372.
[4] A. Gopinath and J. B. Rankin, "GaAs FET RF switches," *IEEE Trans. Electron Devices*, vol. ED-32, pp. 1272–1278, July 1985.
[5] J. F. White, *Semiconductor Control.* Dedham, MA: Artech House, 1977, ch. 5.
[6] T. Takada, K. Yokoyama, M. Ida, and T. Sudo, "A MESFET variable-capacitance model for GaAs integrated circuit simulation," *IEEE Trans. Microwave Theory Tech.*, vol. MTT-30, pp. 719–724, May 1982.
[7] R. E. Neidert and C. J. Scott, "Computer program for microwave MESFET modeling," NRL Report 8561, Feb. 1982.
[8] V. Sokolov, J. J. Gedder, A. Contolatis, P. E. Bauhahan, and C. Chao, "A K_a-band GaAs monolithic phase shifter," *IEEE Trans. Microwave Theory Tech.* vol. MTT-31, pp. 1077–1083, Dec. 1983.
[9] M. Hagio, S. Katsu, M. Kazumura, and G. Kano, "A new self-align technology for GaAs analog MMIC's," *IEEE Trans. Electron Devices*, vol. ED-33, pp. 754–758, June 1986.



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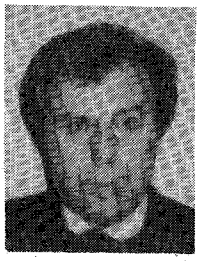

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